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Analog Neural Network Model based on Logarithmic Four-Quadrant Multipliers

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Abstract

Models for artificial intelligence, machine learning, and neural networks are implemented on digital computers with a von Neumann architecture. Few studies have considered analog neural networks. In our previous study, we used multipliers for representing connecting weights in a neural network. The multipliers calculate the product of input signals and their corresponding connecting weights. However, their operating range is limited by semiconductor characteristics. The input and output ranges for networks that use these multipliers are thus limited. Furthermore, the circuit operation becomes unstable. Here, we propose a logarithmic four-quadrant multiplier for representing connecting weights. Experiments show that this multiplier exhibits stable operation over a wide range. A model that uses only analog electronic circuits is presented. Its learning time is quite short compared to that for models implemented on a digital computer. We increased the number of units and network layers. We suggest the possibility of a hardware implementation of a deep learning model.

Keywords: Logarithmic Circuit, Multiplier, Neural Network.

1 Introduction

Multilayer neural network models, particularly deep learning models, have been extensively researched. Their performance has been greatly improved for image and sound recognition. However, these models run on general purpose computers with a von Neumann architecture. A few studies have constructed an analog parallel hardware structure based on a biological information processing mechanism. Many models have been proposed for image recognition and phenomenon prediction. Hardware realizations of some models have been achieved using large-scale parallel computers.

In this study, we propose a logarithmic four-quadrant multiplier for representing connecting weights in a neural network. Experiments are conducted to show that the multiplier can stably

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operate over a wide range. A neural network model based on only analog electronic circuits is presented. The learning time is quite short compared to that for models implemented on a digital computer. In addition, we expand the multipliers from one quadrant to four quadrants realized only with analog circuits.

The motivation is fusion of two types of technology, biological system and analog circuit technology. The proposed model is expected to be suitable for application in various sensors with a completely new concept. And it also expects improving the performance of intelligent mechanical systems. In addition, the proposed model offers excellent fault tolerance.

1.1 Analog Hardware Neural Network

The main advantage of an analog machine learning network is that its operation is realized by a real-time linear system, and thus is not influenced by clock frequency behavior. There have been some proposals for analog neural network models [1-2]. In an analog circuit, one element is used for the implementation of the analog data saving unit, keeping the analog numerical value for a while using analog memory [3]. Dynamic random access memory (DRAM) can store data for a short period of time [4]. However, when the charge is maintained for a long time in a capacitor, the processing system needs to keep the numerical value data in memory, and a refresh process is required. The electric charge in capacitors decreases over time. It is not difficult to recover the electric charge of a capacitor by a refresh process in general digital binary memory. In contrast, for analog memory, a refresh process is difficult because linear analog data is stored, and it needs a time analysis system based on an electric charge reduction curve. Studies have proposed memory methods for connecting weights in neural networks, such as floating gate type devices [5] and magnetic storage [6].

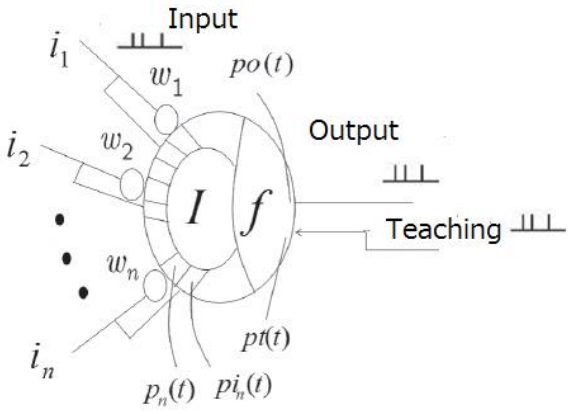

Figure 1: Pulsed neuron model

1.2 Pulsed Neural Network

In a pulsed neural network, the number of pulses, used as learning data, change the connecting weights, as shown in Fig. 1. Such networks can maintain their connecting weights after learning [7]. However, they require a long time for learning because a large number of pulses are required. For example, if the average pulse duration is 10μs and 100 pulses are needed for learning, the process will take approximately 1ms.

1.3 Variable Connecting Weights

Early analog hardware neural network models were built using operational amplifiers and resistors. However, the connecting weights (resistance values) for the learning process were difficult to change because fixed resistors were used. In our previous study, we proposed a movement detection biological vision model that uses analog general electronic circuits. The model had four layers, each of which had a differentiation circuit, a difference circuit, and multipliers for detecting motion output. This model can be used to examine artificial vision systems. It was shown to detect the target object and its motion and velocity in a simulation using an analog network electric circuit [8-9]. There was an attempt to realize a multilayer hardware neural network using analog electronic circuits. Models in the machine learning and neural network fields are implemented on a digital computer. Few studies have considered analog learning neural networks.

In a previous study, a hardware neural network was built using variable resistors for representing the connecting weights. In the learning process, each resistance value had to be adjusted by hand. In another study, multipliers were used for representing the connecting weights. The multipliers calculate the product of the input signal and the corresponding connecting weight. In a different study, a three-layer neural network based on analog circuits was designed. The model used multipliers that consisted of an operational amplifier and a metal-oxide-semiconductor field-effect transistor (MOSFET) for representing the connecting weights. The connecting weights could be easily varied by controlling the input signal. The model had three layers with two input units and one output unit. After the learning process, the model worked exclusive OR logic in a SPICE simulation, and was a linear inseparable problem [10-11].

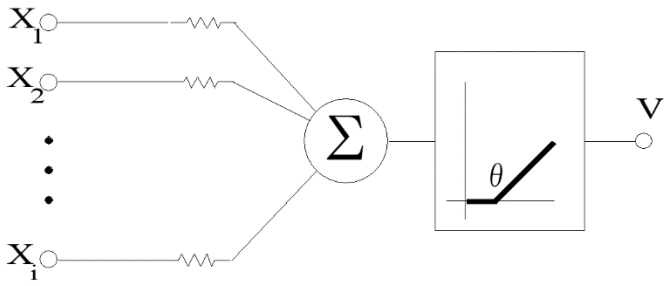

Figure 2: Neuron model based on fixed resistors

2 Neural Network based on Analog Electronic Circuit

2.1 Neural Network based on Fixed or Variable Resistors

Early analog neural circuits models were built using adder circuits, threshold circuit, and fixed resistors, as shown in Fig. 2. A previous study [12] built a hardware neural network using variable resistors, whose resistances represented the connecting weights for the network. The network, which had nine units in the input layer, three units in the middle layer, and three units in the

output layer, could recognize simple patterns. However, in the learning process, each resistance value had to be adjusted by hand.

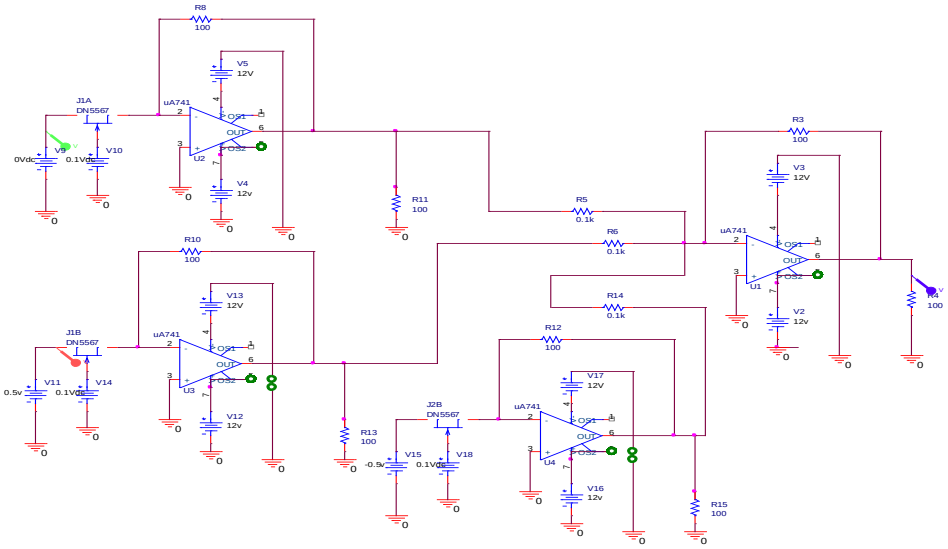

Figure 3: Neuron model based on multipliers

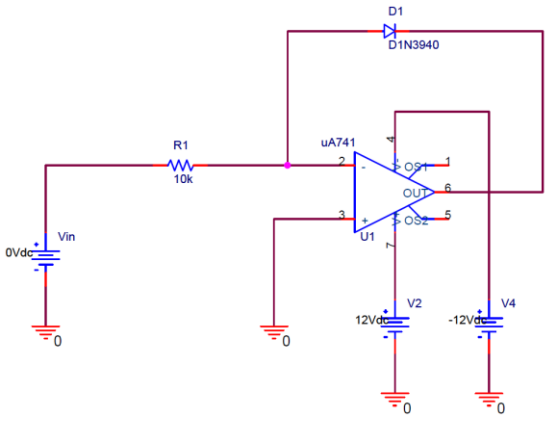

Figure 4: Simple logarithmic conversion circuit

2.2 Neural Network based on Multipliers

In our previous study, multipliers were used for representing the connecting weights, which could be easily changed by controlling the input signal. Figure 3 shows a two-input and one-output neural circuit that represents the structure of one neuron. There are three input units, two input signals, and one threshold value. The input unit calculates the product of the input signal and the corresponding connecting weight. The connecting weights can be easily changed by changing the voltage of the MOSFET gate signal. A learning neural network was constructed. It is a basic perceptron model with a two-input unit, a one-output unit, and a feedback circuit. Figure 3 also shows the perceptron network based on an analog electronic circuit [14].

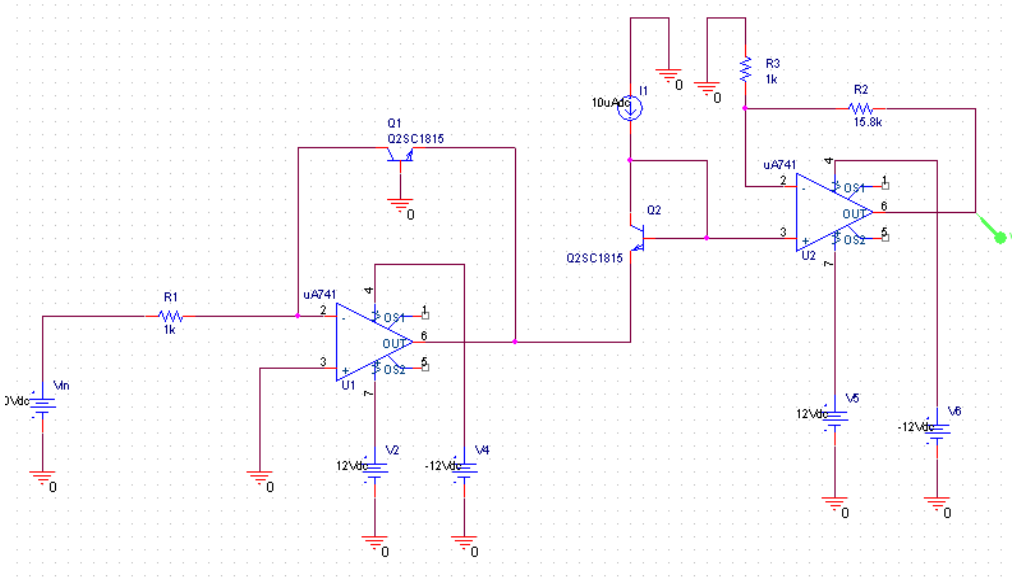

Figure 5: Improved logarithmic conversion circuit

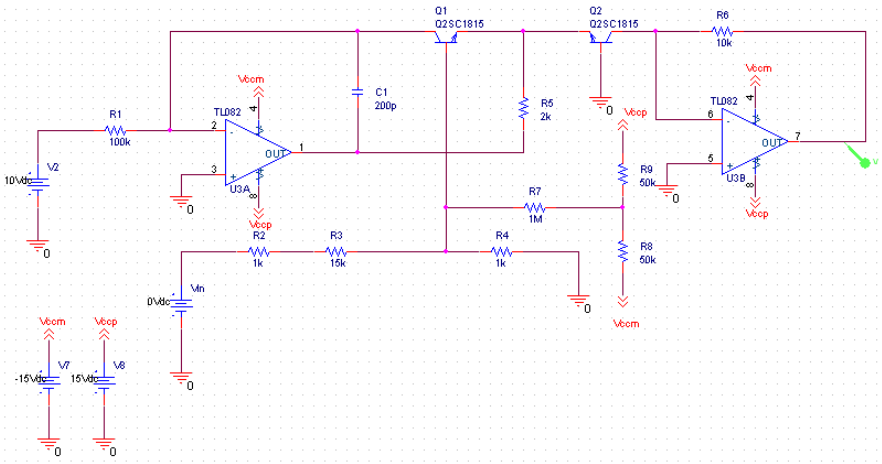

Figure 6: Inverse logarithmic conversion circuit (exponential conversion circuit)

3 Logarithmic Four-Quadrant Multiplier

For the hardware learning network described above, the operating ranges of the input and output voltages are limited. Moreover, the circuit behavior is sometimes unstable because the multiplier uses semiconductors, which have manufacturing variance and an output voltage limitation. To overcome these problems, we propose a logarithmic four-quadrant multiplier for representing connecting weights. The multiplier is composed of a logarithmic circuit, an adder, an exponential circuit (inverse logarithmic circuit), an inverse circuit, a comparator, an absolute value circuit, and an analog switch. Its operation is more stable than that for existing models and it has a wide operating range.

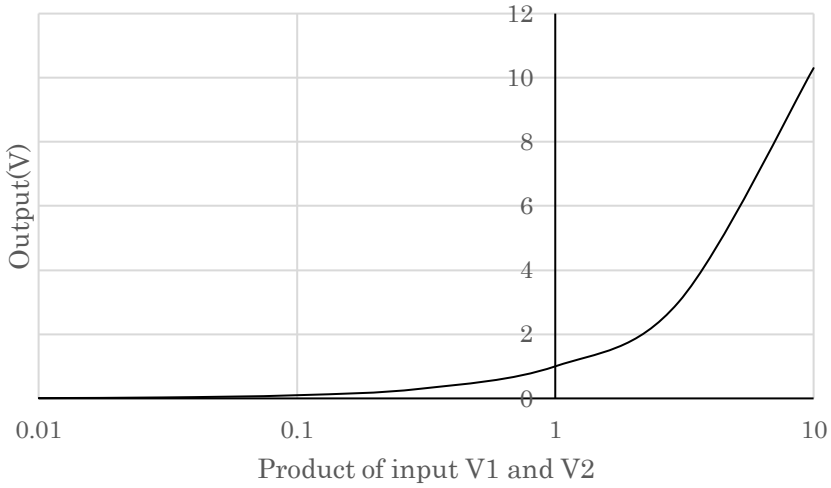

Figure 7: Simulation results for logarithmic multiplier

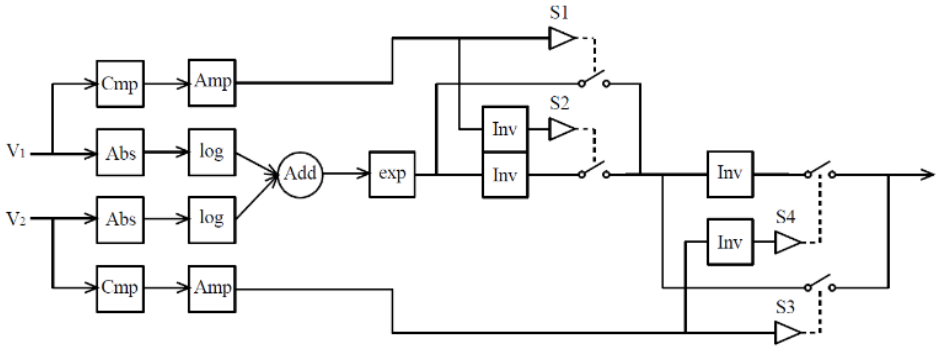

Figure 8: Diagram of logarithmic four-quadrant multiplier

3.1 Logarithmic Circuit and Inverse Logarithmic Circuit

A simple logarithmic conversion circuit is shown in Fig. 4. This circuit uses a diode for the feedback section. However, its operating range is very small, and the input and output voltage ranges for the network are thus limited. In this experiment, we used an improved logarithmic conversion circuit, which is shown in Fig. 5. When the base-emitter potential of the two transistors is small, the output is proportional to the logarithmic ratio of the collector currents between the two transistors. The first-stage operational amplifier performs logarithmic conversion. Because the base-emitter voltage for the first-stage transistor cannot be increased, the second-stage operational amplifier outputs the amplified signal from the first-stage operational

amplifier. The inverse logarithmic conversion circuit (exponential conversion circuit) is shown in Fig. 6.

3.2 Logarithmic Multiplier

The mechanism for the proposed multiplier is as follows. First, two logarithmically converted signals are input to the adder. Next, the output of the adder is input to the inverse logarithmic conversion circuit. The output is the product of the two original input signals. This logarithmic multiplier is more stable than our previous multiplier circuit. Figure 7 shows the simulation results for the logarithmic multiplier. The horizontal axis is the product of the input voltages on a logarithmic scale. The vertical axis is the output voltage. Although there is a slight error, the multiplication circuit can operate in a wide voltage range. However, the input voltage must be positive because of the logarithmic characteristics. To realize a neural network, a four-quadrant multiplier is required.

3.3 Logarithmic Four-Quadrant Multiplier

Figure 8 shows a diagram of the proposed logarithmic four-quadrant multiplier. It is composed of a logarithmic circuit, an adder circuit, an exponential circuit, an inverse circuit, a comparator, an absolute value circuit, and an analog switch. First, input voltages V_1 and V_2 are converted to positive values by the absolute value circuit. Next, the positive values are input to the logarithmic conversion circuit. The logarithmic values are input to the adder. The output of the adder is input to the inverse logarithmic conversion circuit (exponential function circuit). The output of the exponential function circuit is equal to the absolute value of the product of inputs V_1 and V_2.

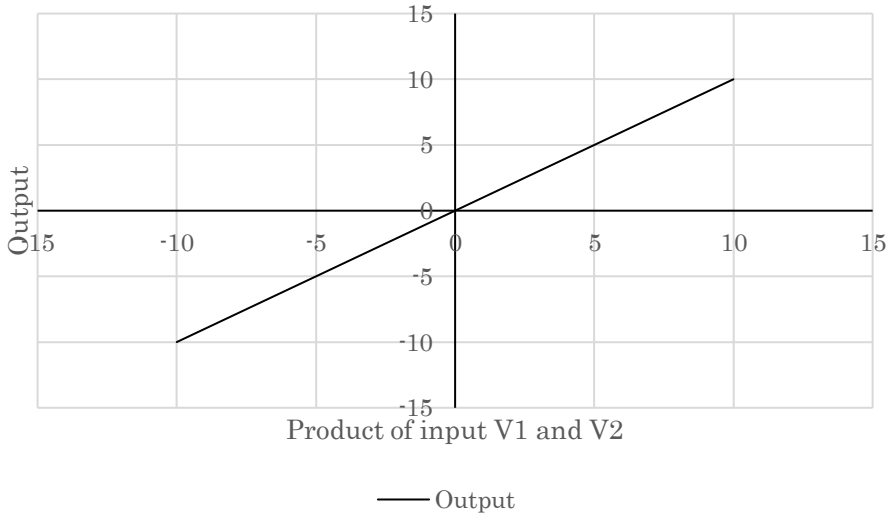

Figure 9: Simulation results for logarithmic four-quadrant multiplier

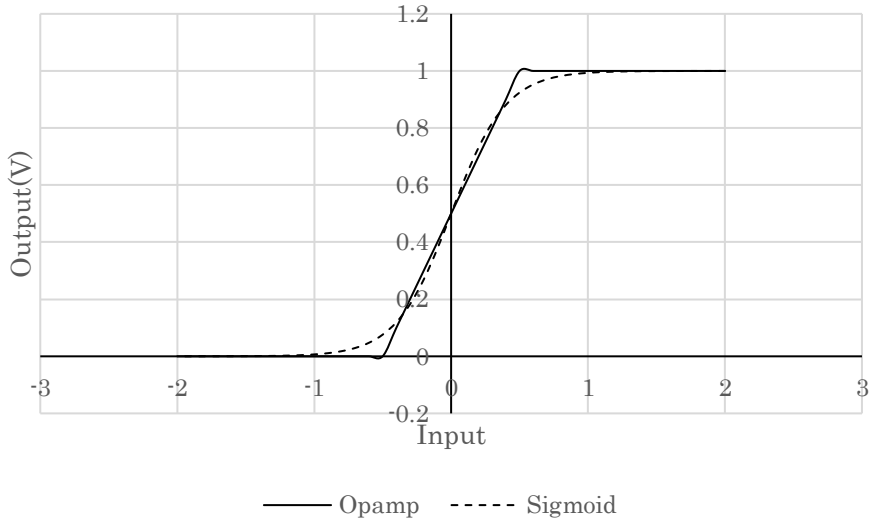

Figure 10: Outputs of operational amplifier and sigmoid function

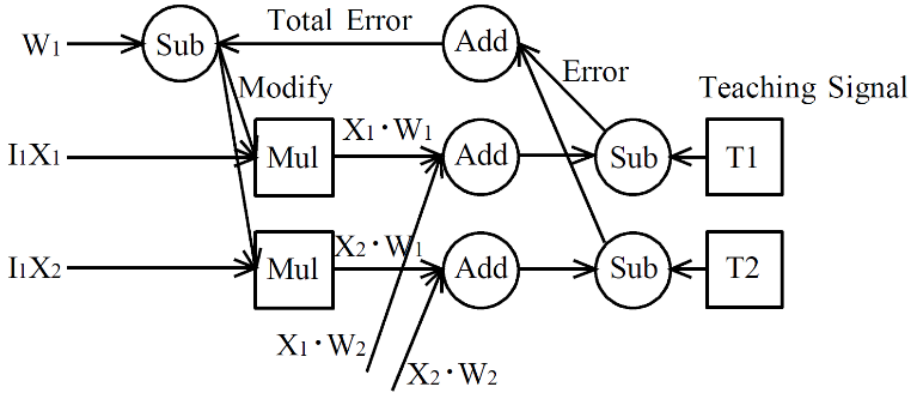

Figure 11: Structure of two-input, one-output, two-pattern, and three-layer analog neural network

Inputs V_1 and V_2 are also input to the comparison circuit. The comparison circuit compares the ground voltage and the input voltage. If the input voltage is positive (negative), a positive (negative) constant value is output. The output of the comparison circuit becomes the input of the amplifier circuit. This circuit amplifies the operating voltage of the next-stage analog switch. If V_1 is positive, analog switch S_1 is turned on and the output of the exponential function circuit is fed to the next stage. If V_2 is negative, analog switch S_2 is turned on and the output of the exponential function circuit is inverted and fed to the next stage. Thus, the output of the analog switch is the product of V_1 and V_2, and the positive and negative signs are the same as that of V_1. In the same way, for analog switches S_3 and S_4, if the value of V_1 is positive, the current is fed to the output. Alternatively, if the value of V_2 is negative, the current is inverted and fed to the output. Finally, the output is the product of inputs V_1 and V_2. This circuit operates as a four-quadrant multiplier [14].

Figure 9 shows the simulation results for the logarithmic four-quadrant multiplier. The horizontal axis is the product of the input voltages. The vertical axis is the output voltage. The graph is a straight line. Although there is a slight error, the four-quadrant multiplier can operate in a wide voltage range. In our previous research, the input operating voltage was in the range of approximately ± 200 mV and the output operating voltage was in the range of approximately ± 1V in the reason of circuit limitation [15]. However, Figure 9 shows the both input and output operating voltage was in the range of approximately ±10V. The wide operating voltage range gives this circuit excellent stability. Moreover, the output value of this model is the output voltage of this circuit. We don't need to convert the data; we can use the raw data from this model for practical use.

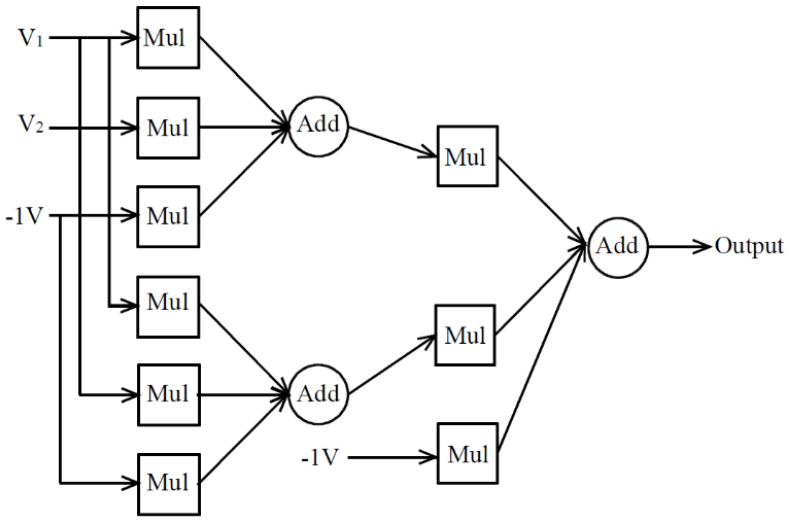

Figure 12: Three-layer neural network

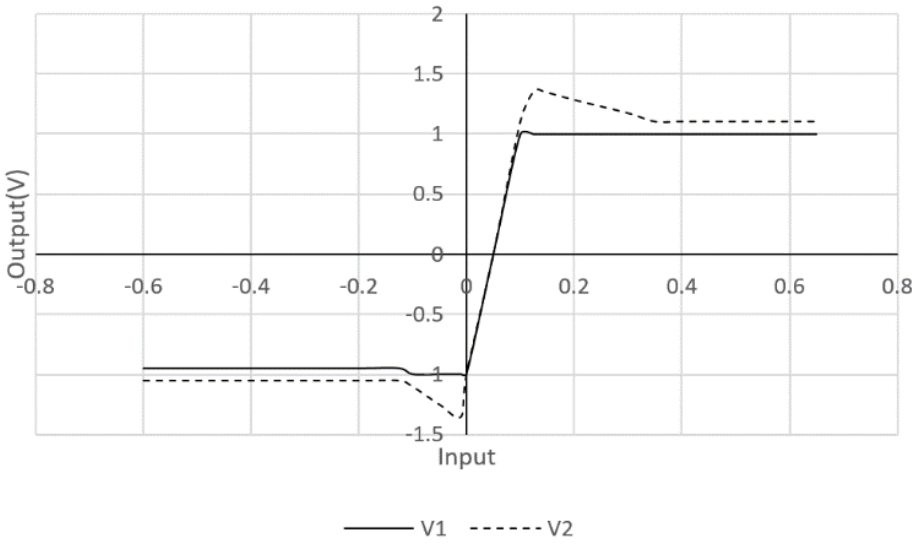

Figure 13: Experimental results for three-layer neural circuit

3.4 Activation Function of Proposed Neural Network

The proposed circuit is based on operational amplifiers. The activation function of a neural network can be approximated by an operational amplifier. Figure 10 shows the characteristics of an operational amplifier and a sigmoid function, which is a typical activation function. The output of the operational amplifier is similar to that of the sigmoid function [14].

3.5 Logarithmic Multiplier

We designed a feedback circuit for neural networks, as shown in Fig. 11. Each teaching signal (T_1 and T_2) has a separate neural network. This model allows real-time learning. In Fig. 11, "Mul", "Add", and "Sub" respectively denote a multiplier, an adder, and a subtractor. This figure shows only the learning feedback part of the back-propagation network. There are two input lines, I_1. I_1X_1 and I_1X_2 are learning patterns. In the adder, the products of the multiplier, X_1W_1 and X_1W_2, are added. The products X_2W_1 and X_2W_2 are also added. Next, the subtractor calculates the error between the output of the adder and the teaching signal. Finally, another subtractor calculates the original connecting weight and the total error. This subtractor outputs the new connecting weights. The simplified figure shows one input signal, one output signal, and two kinds of learning pattern.

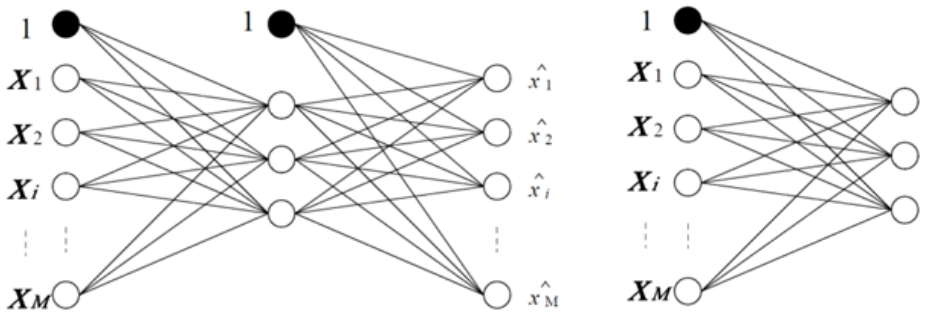

Figure 14: Auto-encoder training and removal of decoding part of stacked auto-encoder

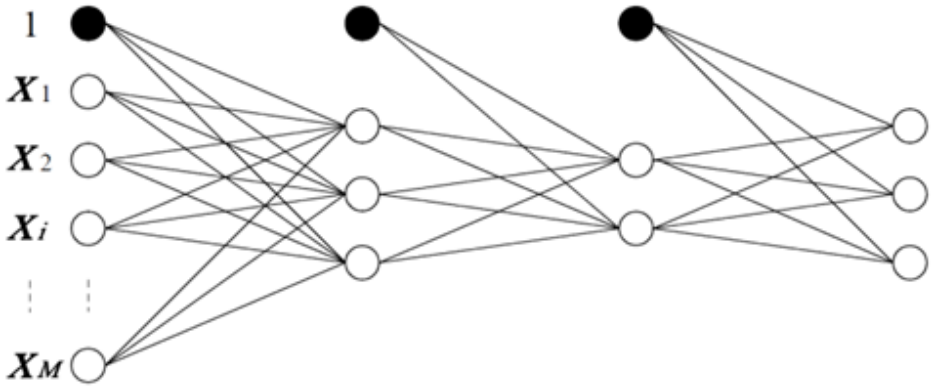

Figure 15: Compressed internal representation

4 Three-Layer Neural Network

We constructed a three-layer neural network that consisted of an input layer (two input units), a middle layer (two middle units), and an output layer (one output unit). We used the neural unit described in the previous section. Figure 12 shows a simplified block diagram of a general neural network model, where the connecting weight part and the feedback part are omitted. The multiplier is used to easily change the connecting weight. In the figure, "Mul" and "Add" respectively denote a multiplier and adder. Due to the characteristics of the circuit, one unit is required for each learning pattern. The model shown in Fig. 10 has two input patterns and two learning patterns.

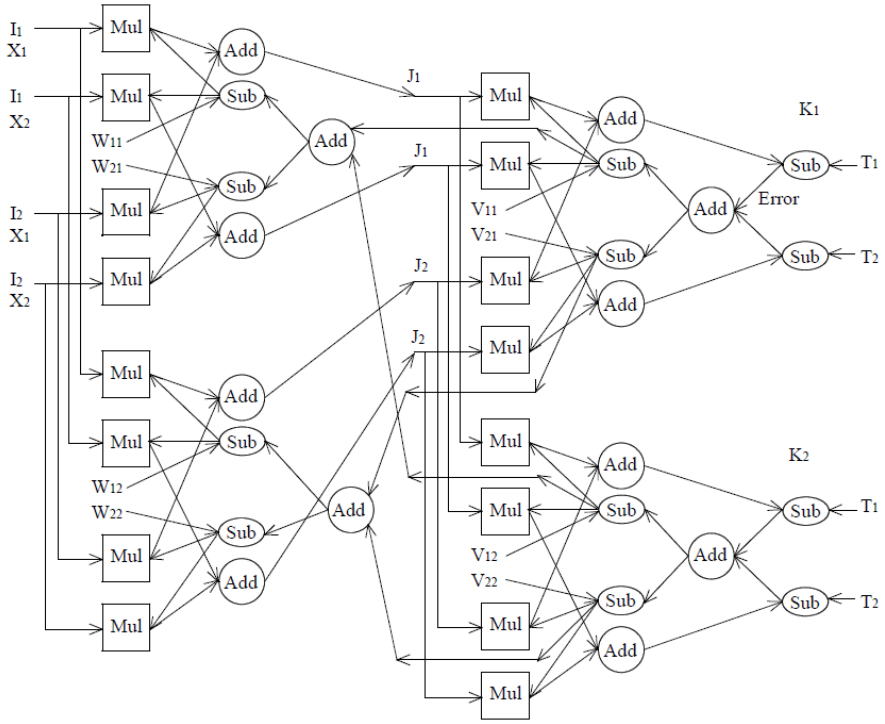

Figure 16: Structure of two-input, one-output, two-pattern, and three-layer analog neural network

The experimental results are shown in Fig. 13. When the voltage was between -0.05 V and 0.15 V, this circuit operated normally. The solid line is the output of the middle layer and the dotted line is the output of the final layer in Fig. 11 [11]. The middle layer outputs a good signal. The output layer outputs a slightly distorted signal, but this is not a significant problem.

5 Deep Learning Model

Deep learning algorithms attempt to categorize data using multiple nonlinear transformations and machine learning. They are applied in image recognition and speech recognition. A general deep learning network structure has nine layers with three superimposed subnetworks (e.g., convolutional networks). A previous study [13] trained such a network

using 10 million images extracted from 10 million YouTube clips. Each subnetwork was trained using the unsupervised stacked auto-encoder method. The neurons responded specifically to various kinds of object, such as human faces, cat faces, and drink bottles.

5.1 Stacked Auto-Encoder

The stacked auto-encoder method is a pre-learning method for networks with a large number of layers. A deep-layer network can be constructed as follows. After the network is trained using the stacked auto-encoder, the decoding part (output layer) of the stacked auto-encoder is removed and the coding part (input and intermediate layers) is kept, as shown in Fig. 14. The obtained network converts an input signal to a compressed information representation, as shown in Fig. 15. Moreover, a more compressed internal representation is obtained and used as the input signal for auto-encoder learning. A multilayer hierarchical network, called a stacked auto-encoder, is thus obtained, where learning and stacking of the encoding part are recursively repeated. For this multilayer network, to add the identified network using the output of the final layer, a supervised learning method is proposed.
In previous research, we described a dynamic neural network learning model. However, this model had only one input unit and one output unit. To realize a hardware deep-learning model, we increased the number of units in each layer, as shown in Fig. 16. Figure 16 shows the structure of a two-input, two-output, two-pattern, and three-layer analog neural network. There are two input lines, I_1. X_1 and X_2 are two learning patterns. These simplified figures show one input signal and two learning patterns. This model suggests the possibility of a hardware implementation of the deep learning model.

6 Conclusion and Future Work

6.1 Conclusion

We proposed a logarithmic four-quadrant multiplier for representing connecting weights in a neural network. The multiplier is composed of a logarithmic circuit, an adder circuit, an exponential circuit, an inverse circuit, a comparator, an absolute value circuit, and an analog switch. Its operation is more stable than that for previous models and it has a wide operating voltage range.

We constructed a three-layer neural network that consists of two input units, two middle units, and one output unit. We confirmed the operatio n of the three-layer analog neural network using a SPICE simulation. The connection weights can be changed by controlling the input voltage, making the network extremely flexible. When the analog neural network is operated, the synapse weight is especially important. To solve this problem, it is necessary to apply a back-propagation rule, which is a general learning rule for multiple electronic circuits. The neural circuit model, which has a fast learning speed and is based on the biological neuron model, can be applied for learning. The proposed model can be applied to analog sensors with soft information processing and is expected to be suitable for application in biomedical sensors, robotics sensors, and control mechanisms.

Deep learning models are commonly used for image and sound recognition. A high-performance artificial intelligence model based on a learning system that uses analog circuits is expected to be

developed in the near future. A deep learning method has been proposed recently [13]. If this method improved toward the deep learning model, many applications will be realized. It is a kind of algorithms in the learning model. The method attempts to categorize data using multiple nonlinear transformations and machine learning. In the fields of image recognition and speech recognition, deep learning methods have attracted attention. We suggest the possibility of a hardware implementation of the deep learning model. This will improve the artificial intelligence element with self-dynamical learning. The realization of an integration device will enable the learning time to be reduced. The proposed model is robust to fault tolerance. Future tasks include system construction and large-scale integration [16].

6.2 Future Prospects of Deep Learning Model

The recognition performance of deep learning models has continued to improve. Such models can be applied to self-driving, robotics, and artificial intelligence. The original back propagation learning neural network had a three-layer structure. Currently, deep learning models have nine layers, with three-layer subnetworks [17]. The stacked auto-encoder algorithm can detect feature data and abstract expression data from input images using a large quantity of learning data. The proposed logarithmic four-quadrant multiplier enables the development of a flexible neural network structure such as a deep learning model [18-19]. Increasing the number of units, large-scale system development, and creating integrated circuits are problems for future research [20-21].

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